**METHOD AND SYSTEM FOR PREVENTING NVRAM CORRUPTION**

**INVENTOR (S):**

**JAMES A. RANLETT**

ABSTRACT OF THE DISCLOSURE

A system and method for minimizing memory corruption at power up and/or reset is provided. The system includes, a digitally controlled potentiometer between an adapter and the memory; and a voltage divider functionally coupled to the potentiometer. The voltage divider includes a pull-down resistor that brings down the voltage at one of the plural potentiometer pins, minimizing the chances of memory corruption at power up and/or reset. The method includes, setting the potentiometer to a resistance value such that upon power up and/or reset data cannot be written to the memory; and setting the potentiometer in an increment or decrement mode such that resistance between plural pins of the potentiometer can be increased or decreased allowing content to be written to the memory after power up and/or reset.